47. The pair of capacitors of claim 46, wherein each plug comprises polysilicon and extends through the plate.

48. The capacitors of claim 46, wherein the lower plates are formed from conductive polysilicon.

49. The pair of capacitors of claim 46, wherein the pair of stacked capacitors are coated with a capacitor dielectric layer.

50. A pair of adjacent stacked capacitors fabricated on a semiconductor substrate using a process having a characteristic minimum lithographic feature dimension, the adjacent stacked capacitors respectively including a lower plate having a minimum lateral spacing from one another which is less than the minimum lithographic feature dimension, wherein each of the pair of capacitors comprises:

a plug having a diameter less than the minimum lithographic feature dimension; and

in cross-section, at least two laterally opposed fins interconnected with and projecting laterally from the plug.

51. The pair of capacitors of claim 50, wherein the plug and fins are formed from conductive polysilicon.

52. The pair of capacitors of claim 50, wherein the pair of stacked capacitors are coated with a capacitor dielectric layer.

53. A pair of adjacent stacked capacitors fabricated on a semiconductor substrate using a lithographic process having a characteristic minimum lithographic feature dimension, the adjacent stacked capacitors respectively including a lower plate having a minimum lateral spacing from one another which is less than the minimum lithographic feature dimension, each lower plate comprising a conductive plug having a diameter less than the minimum lithographic feature dimension, and, in cross-section, at least two laterally opposed fins interconnected with and projecting laterally from the plug.

54. The pair of capacitors of claim 53, wherein the plug includes a minimum width which is less than the minimum lithographic feature dimension.

55. The pair of capacitors of claim 53, wherein the plug and fins are formed from conductive polysilicon.

56. The pair of capacitors of claim 53, wherein the pair of stacked capacitors are coated with a capacitor dielectric layer.

57. A pair of adjacent stacked capacitors fabricated on a semiconductor substrate using a lithographic process having a characteristic minimum lithographic feature dimension, the adjacent stacked capacitors respectively including a finned lower plate having a minimum lateral spacing from one another which is less than the minimum lithographic feature dimension, wherein each finned lower plate comprises:

a conductive plug; and

in cross-section, at least two laterally opposed fins interconnected with and projecting laterally from the plug, the plug having a minimum width which is less than the minimum lithographic feature dimension.

58. The pair of capacitors of claim 58, wherein the plug and lower plates are formed from conductive polysilicon.

59. The pair of capacitors of claim 58, wherein the plug and fins are formed from conductive polysilicon.

60. The pair of capacitors of claim 58, wherein the pair of stacked capacitors are coated with a capacitor dielectric layer.